Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

What is claimed is:

1-28. (Canceled)

29. (New) A method comprising:

designing a clock distribution tree for a plurality of circuit components on an integrated circuit to achieve a predetermined clock skew across combinable circuit components of the plurality of circuit components and component blocks of the combinable circuit components;

if the integrated circuit is functional in view of the clock skew, for at least one of the combinable circuit components,

generating a master clock signal and at least one other clock signal transmitted through the clock distribution tree to the circuit component, the circuit component receiving the master clock signal at a first component block of the circuit component;

defining two signal paths including a default path and a bypass path, wherein defining the bypass path includes allowing a second component block of the circuit component to receive the master clock signal and defining the default path includes allowing the second component block of the circuit component to receive the circuit component clock signal; and

wherein during functionality testing, the integrated circuit is tested to determine if the integrated circuit functions utilizing the bypass path, and, if so, the bypass path of the bypass logic is selectable such that the first and second component blocks of the circuit component are controlled by a common clock domain in response to the master clock signal so that signals can be passed between the first and second component blocks.

30. (New) The method of claim 29, further comprising determining if the integrated circuit is functional, with the bypass path and, if not,

selecting the default path.

31. (New) The method of claim 29, wherein the default path is selectable by a user.

32. (New) The method of claim 29, wherein the bypass path is selectable by a user.

33. (New) The method of claim 29, wherein selecting the bypass path further includes utilizing software to write a bit to a clocking register to instruct the at least one circuit component to use the bypass path.

34. (New) The method of claim 29, wherein the bypass path includes bypass logic having a bypass switch located in the second component block of the at least one circuit component.

35. (New) The method of claim 34, wherein the bypass switch is responsive to a bypass activation signal to activate the bypass path.

36. (New) The method of claim 29, wherein the default path is automatically selected when the integrated circuit powers up.

37. (New) A method comprising:

designing a plurality of circuit components on an integrated circuit to achieve a clock skew less than a predetermined minimum;

designing a clock distribution tree for the plurality of circuit components on the integrated circuit to achieve the clock skew across combinable circuit components of the plurality of circuit components and component blocks of the circuit components;

if the integrated circuit is functional in view of the clock skew, for at least one of the combinable circuit components,

generating a master clock signal and at least one other clock signal transmitted through the clock distribution tree to the circuit component, the circuit component receiving the master clock signal at a first component block of the circuit component;

defining two signal paths including a default path and a bypass path, wherein defining the bypass path includes allowing a second component block of the circuit component to receive the master clock signal and defining the default path includes allowing the second component block of the circuit component to receive the circuit component clock signal; and

determining if the integrated circuit is functional with the bypass path and, if not, selecting the default path.

38. (New) The method of claim 37, wherein if the integrated circuit is functional with the bypass path, selecting the bypass path such that the first and second component blocks of the circuit component are controlled by a common clock domain in response to the master clock signal so that signals can be passed between the first and second component blocks.

39. (New) The method of claim 38, wherein the bypass path is selectable by a user.

40. (New) The method of claim 38, wherein selecting the bypass path further includes utilizing software to write a bit to a clocking register to instruct the at least one circuit component to use the bypass path.

41. (New) The method of claim 38, wherein the bypass path includes bypass logic having a bypass switch located in the second component block of the at least one circuit component.

42. (New) The method of claim 41, wherein the bypass switch is responsive to a bypass activation signal to activate the bypass path.

43. (New) The method of claim 37, wherein the default path is selectable by a user.

44. (New) The method of claim 37, wherein the default path is automatically selected when the integrated circuit powers up.